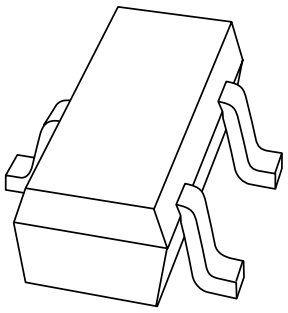
DATA SHEET



PDTC115EE

NPN resistor-equipped transistor;
R1 = 100 kΩ, R2 = 100 kΩ

Product specification

2002 May 08

Philips
Semiconductors

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NPN resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩ

PDTC115EE

FEATURES

- Built-in bias resistors R1 and R2 (typically 100 kΩ each)
- Simplification of circuit design
- Reduces number of components and required PCB area.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configuration without use of external resistors.

DESCRIPTION

NPN resistor-equipped transistor in a SOT416 (SC-75) plastic package.

MARKING

TYPE NUMBER	MARKING CODE
PDTC115EE	46

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	50	V
I_O	output current (DC)	20	mA
R1	bias resistor	100	kΩ
R2	bias resistor	100	kΩ

PINNING

PIN	DESCRIPTION
1	base/input
2	emitter/ground
3	collector/output

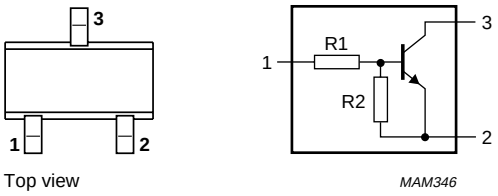


Fig.1 Simplified outline (SOT416) and symbol.

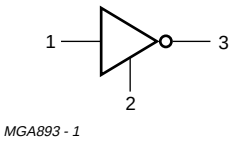


Fig.2 Equivalent inverter symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_i	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I_O	output current (DC)		–	20	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	150	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Refer to standard SOT416 (SC-75) mounting conditions.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air; note 1	833	K/W

Note

1. Refer to standard SOT416 (SC-75) mounting conditions.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

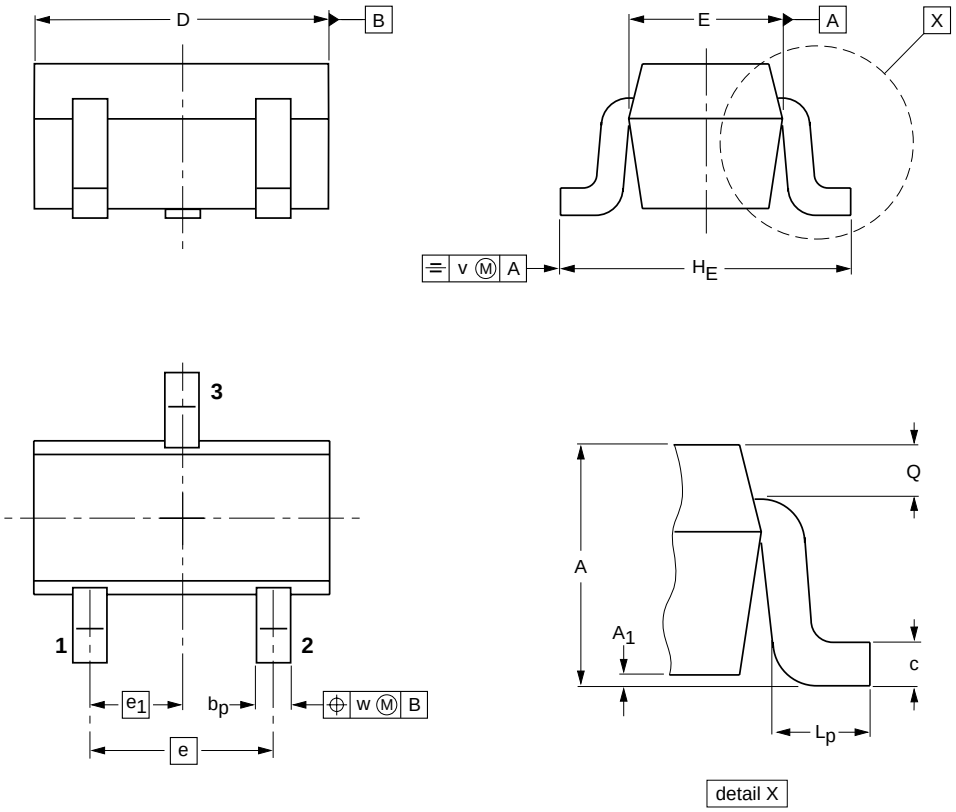
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0	–	–	1	µA
		V_{CE} = 30 V; I_B = 0; T_j = 150 °C	–	–	50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0	–	–	50	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 300 mA; I_B = 10 mA	–	–	150	mV
$V_{i(off)}$	input off voltage	V_{CE} = 5 V; I_C = 100 µA	–	–	0.5	V
$V_{i(on)}$	input on voltage	V_{CE} = 0.3 V; I_C = 1 mA	3	–	–	V
R1	input resistor		70	100	130	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e = 0$; V_{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

NPN resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩ

PDTC115EE

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT416**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
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